WHAT IS CLAIMED IS:

1. A pulse width modulation circuit for driving a full – bridge output load comprising:

a pulse width modulation stage for generating from an input data stream a pulse width modulated data stream for driving a terminal of a full – bridge output load and another pulse width modulated data stream for driving another terminal of the full bridge output load, wherein the another pulse width modulated data stream is a complement of the pulse width modulated data stream; and

delay circuitry for delaying the another pulse width modulated data stream relative to the pulse width modulated data stream such that edges of the another pulse width modulated data stream and edges of the pulse width modulated data stream are temporally spaced.

2. The pulse width modulation circuit of Claim 1, further comprising:

a driver circuit for driving the terminal of the full – bridge output load in response to the pulse width modulated data stream;

another driver circuit for driving the another terminal of the full – bridge output load in response to the another pulse width modulated data stream; and

a power supply having a non – zero output impedance supplying a voltage to the driver circuit and the another driver circuit.

3. The pulse width modulation circuit of Claim 1, wherein the pulse width modulation circuit is a selected one of a plurality of pulse width modulation circuits forming a portion of a multiple-channel signal processing system.

4. The pulse width modulation circuit of Claim 1, wherein the delay circuit comprises a shift register operable to delay the another pulse width modulated data stream by a selected number of periods of a clock signal.

5. The pulse width modulation circuit of Claim 4, wherein the selected number of clock periods of the clock signal is programmable.

6. The pulse width modulation circuit of Claim 4, wherein the clock signal comprises a clock signal utilized by the pulse width modulation stage for generating the pulse width modulated data stream.

7. The pulse width modulation circuit of Claim 1, wherein the delay circuitry is integral to the pulse width modulation stage.

8. A method of driving a full – bridge load comprising:

generating from an input data stream a pulse width modulated data stream for driving a terminal of a full – bridge load and another pulse width modulated data stream for driving another terminal of the full bridge output load, wherein the another pulse width modulated data stream is a complement of the pulse width modulated data stream; and

delaying the another pulse width modulated data stream relative to the pulse width modulated data stream such that edges of the another pulse width modulated data stream and edges of the pulse width modulated data stream are temporally spaced.

9. The method of Claim 8, wherein delaying the another pulse width modulated data stream comprises delaying the another pulse width modulated data by a selected number of periods of a clock signal.

10. The method of Claim 8, wherein in generating the pulse width modulated data stream and the another pulse width modulated data stream is performed in response to a clock signal and delaying the another pulse width modulated data stream comprises delaying the another pulse width modulated data stream by a selected number of periods of the clock signal,

11. The method of Claim 8, selecting a user selectable amount of delay for delaying the another pulse width modulated data stream.

12. The method of Claim 8, wherein the pulse width modulated data stream and the another pulse width pulse data stream are generated from a single power source.

13. An audio circuit comprising:

a data path including:

a pulse width modulation engine for encoding an input signal into an pulse width modulated data stream and an inverse of the pulse width modulated data stream;

a first driver circuit for driving a first node in response to the pulse width modulated data stream;

a second driver circuit for driving a second node in response to the inverse of the pulse width modulated data stream; and

a delay circuit for delaying a selected one of the pulse width modulated data stream and the another pulse width modulated data stream such that edges of the pulse width modulated data stream at the first node are temporally spaced from corresponding edges of the inverse of the pulse width modulated data stream at the second node.

14. The audio circuit of Claim 13, further comprising a noise shaper for generating the input signal to the pulse width modulation engine.

15. The audio circuit of Claim 13, wherein the data path comprises a selected one of a plurality of like data paths.

16. The audio circuit of Claim 13, wherein the delay circuit is programmable to delay the selected one of the pulse width modulated data stream and the inverse of the pulse width modulated data stream by a selected amount

17. The audio circuit of Claim 13, wherein the delay circuit includes a shift register for delaying the selected one of the pulse width modulated data stream and the inverse of the pulse width modulated data stream by a selected number of clock periods of a clock signal.

18. The audio circuit of Claim 13, further comprising a full – bridge load coupled across the first and second nodes.

19. The audio circuit of Claim 18, wherein the full – bridge load comprises an audio speaker.

20. The audio circuit of Claim 13, further comprising a power supply coupled to both the first and second drivers.

21. A pulse-width modulation stage for driving a full-bridge load comprising:

a first path for generating a first pulse-width modulated data stream from an input data stream for driving a first terminal of a full-bridge load;

a second path for generating a second pulse width modulated data stream from the input data stream;

an inverter for inverting the second pulse width modulated data stream; and

a delay stage for delaying by a selected amount an inverted second pulse width modulated data stream output from the inverter, a delayed inverted second pulse-width modulated data stream output from the delay stage for driving a second terminal of the full-bridge load.

22. The pulse-width modulation stage of Claim 21, wherein the first and second paths each comprises a noise shaper and a pulse-width encoder.

23. The pulse-width modulation stage of Claim 21, wherein the first and second paths each comprises a pulse-width modulation encoder.

24. The pulse-width modulation stage of Claim 23, wherein each pulse-width modulation encoder comprises a digital pulse-width modulation encoder.

25. The pulse-width modulation stage of Claim 23, wherein each pulse-width modulation encoder comprises an analog pulse-width modulation encoder.